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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,061	12/30/2003	Justin K. Brask	42P16680	9123

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/750,061	BRASK ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-22 and 26-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-42* is/are allowed.

6)☒ Claim(s) *19-22,26 and 43-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Amendment filed on 8/26/2005.

Currently, claims 19-22 and 26-52 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 19-22, 26 and 43-52 are rejected under 35 U.S.C. 103(a) as being obvious over Chau et al. (U.S. Patent No. 6,858,478 filed 2/14/2003) in view of Nakajima et al (US Pub. No. 2004/0142567 filed 11/6/2003).

The applied reference has a common inventor and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an

invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Chau shows the method substantially as claimed in Figs. 3-5G and corresponding text as: forming a semiconductor body (304) having a top surface and laterally opposite sidewalls on a substrate (302) wherein said semiconductor body has channel region with a p type conductivity (col. 2, line 66-col. 3, line 19) (col. 3, lines 40-52); forming a gate dielectric (322) on said top surface (316) of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body (col. 4, lines 19-36); forming a gate electrode (324) on said gate dielectric and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body, wherein said gate electrode comprises a metal film formed directly adjacent to said gate dielectric (col. 4, lines 37-51); and forming a pair of source/drain regions (330,332) formed in said semiconductor body on opposite sides of said gate electrode (col. 4, line 66-col. 5, line

18) (claim 19). Chau teaches that the gate electrode comprises only said metal film (col. 4, lines 53-65) (claim 20). Chau teaches that the gate electrode further comprises a doped silicon film formed on said metal film (col. 4, lines 53-65) (claim 21). Chau teaches that the gate dielectric is selected from the group consisting of tantalum oxide, titanium oxide, hafnium oxide, zirconium oxide, PZT, BST, aluminum oxide and silicates thereof (col. 4, lines 19-36) (claim 26).

Chau shows the method substantially as claimed in Figs. 3-5G and corresponding text as: forming a semiconductor body (304) having a top surface and laterally opposite sidewalls on a substrate (302) wherein said semiconductor body has channel region with a n type conductivity (col. 2, line 66-col. 3, line 19) (col. 3, lines 40-52); forming a gate dielectric (322) on said top surface (316) of said semiconductor body and on said laterally opposite sidewalls of said semiconductor body (col. 4, lines 19-36); forming a gate electrode (324) on said gate dielectric and adjacent to said gate dielectric on said laterally opposite sidewalls of said semiconductor body, wherein said gate electrode comprises a metal film formed directly adjacent to said gate dielectric (col. 4, lines 37-51); and forming a pair of source/drain regions (330,332) formed in said semiconductor body on opposite sides of said gate electrode (col. 4, line 66-col. 5, line 18) (claim 43). Chau teaches that the gate electrode comprises only said metal film (col. 4, lines 53-65) (claim 44). Chau teaches that the gate electrode further comprises a doped silicon film formed on said metal film (col. 4, lines 53-65) (claim 45). Chau teaches that the gate dielectric is selected from the group consisting of tantalum oxide,

titanium oxide, hafnium oxide, zirconium oxide, PZT, BST, aluminum oxide and silicates thereof (col. 4, lines 19-36) (claim 47).

Chau shows the method substantially as claimed in Figs. 3-5G and corresponding text as: forming a first semiconductor body having a top surface and laterally opposite sidewalls on a substrate, wherein said first semiconductor body has a channel region with an n type conductivity and forming a second semiconductor body having a top surface and laterally opposite sidewalls on said substrate, wherein said second semiconductor body has a channel region with an n type conductivity (col. 2, line 66-col. 3, line 19); forming a first gate electrode on said first gate dielectric layer wherein said first gate electrode includes a first metal film formed directly on said first gate dielectric layer and forming a second gate electrode on said second gate dielectric layer wherein said second gate electrode has a second metal film formed directly on said gate dielectric layer (col. 4, lines 37-51); and forming a first pair of source/drain region in said first semiconductor body on opposite sides of said first gate electrode and forming a second pair of source/drain regions in said second semiconductor body on opposite sides of said second gate electrode (col. 4, line 66-col. 5, line 18) (claim 48). Chau teaches that the first gate electrode comprises only said metal film and the second gate electrode comprises only said second metal film (col. 4, lines 53-65) (claim 49). Chau teaches that the first gate electrode and said second gate electrode further comprises a doped silicon film formed on said first metal film and the second metal film (col. 4, lines 53-65) (claim 50). Chau teaches that the gate dielectric is selected from

the group consisting of tantalum oxide, titanium oxide, hafnium oxide, zirconium oxide, PZT, BST, aluminum oxide and silicates thereof (col. 4, lines 19-36) (claim 52).

Chau lacks anticipation only in not explicitly teaching that: 1) in the semiconductor body is silicon, and said source/drain regions have a p-type conductivity and said metal film has a work function between 4.9 eV and 5.2 eV (claim 19); 2) the metal film is formed to a thickness between 25-100Å and said doped silicon film is formed to a thickness between 500-3000Å (claims 22, 46 and 51); 3) in the semiconductor body is silicon, and said source/drain regions have a n-type conductivity and said metal film has a work function between 3.9 eV and 4.2 eV (claim 43); and 4) forming a first gate electrode on said first gate dielectric layer wherein said first gate electrode includes a first metal film formed directly on said first gate dielectric layer with a work function between 3.9-4.2 eV and forming a second gate electrode on said second gate dielectric layer wherein said second gate electrode has a second metal film formed directly on said gate dielectric layer with a work function between 4.9-5.2 eV (claim 48).

a. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon

another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575,1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Nakajima shows a semiconductor device that contains a metal layer with a work function that is dependent upon the dopant concentration of the substrate. For an n-type semiconductor has a metal formed with a work function in the range of 4.0 eV to 4.2 eV [0007]. The work function of the metal in the p-type semiconductor is in the range of about 4.9 eV to 5.1 eV [0007]. These ranges help to accomplish good ohmic contact.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Chau by having the work function depend on the dopant conductivity in the substrate, as taught by Nakajima, with the motivation that Nakajima teaches that the ranges help to accomplish good ohmic contact.

Allowable Subject Matter

4. Claims 27-42 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...blanket depositing a second gate electrode material on said second gate dielectric layer in said second opening on said top surface of said second semiconductor body and adjacent to said second gate dielectric layer on said sidewalls of said semiconductor body, wherein said second gate electrode material comprises a

second metal film formed directly on said gate dielectric layer wherein said second metal film is different than said first metal layer, as required by claims 27 and 38.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

5. Applicant's arguments with respect to claims 19-22 and 26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
November 9, 2006